2133

PATENT
5181-94400/P6301

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/037,361
Filed: October 29, 2001
Inventor:
James M. Byrd

Title: System and Method for Verifying Error Detection/Correction Logic

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Examiner: Gandhi, Dipakkumar B.
Group/Art Unit: 2133
Atty. Dkt. No: 5181-94400

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Robert C. Kowert
Printed Name

Signature

October 27, 2004
Date

RESPONSE TO OFFICE ACTION OF JULY 28, 2004

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Office Action of July 28, 2004, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.